IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Appellant:	Yu
Filing Date:	January 3, 2000
For:	MOS TRANSISTOR WITH ASYMMETRICAL SOURCE/DRAIN EXTENSIONS
Group Art Unit:	2815
Docket No.:	39153/223
Application No.:	09/476,961
Examiner:	Warren, M.

BRIEF ON APPEAL

Box AF
Commissioner for Patents
Washington, DC 20231

Sir:

REAL PARTY IN INTEREST

This application was assigned to Advanced Micro Devices, Inc. having a place of business at One AMD Place, 1160 Kern Avenue, Sunnyvale, CA 94086.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF THE CLAIMS

This is an appeal from the Final Office Action mailed April 24, 2002, finally rejecting Claims 18-37 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,677,224 (Kadosh et al.). No claims have been allowed. Claims 18-37 are the subject of the present appeal.

STATUS OF THE AMENDMENTS

In response to the Final Office Action, the Applicant submitted Remarks dated June 24, 2002 with arguments traversing the rejection of claims 18-37 under 35 U.S.C. § 103(a) and requesting reconsideration of the application. In an Advisory Action dated July

10, 2002, the Examiner stated "the request for reconsideration does not place the application in condition for allowance because the arguments were not persuasive." No amendment has been filed subsequent to the Advisory Action.

SUMMARY OF THE INVENTION

The present invention relates to integrated circuits and in particular to a transistor having asymmetrical source/drain extensions and methods for manufacturing the same. (Specification, page 1, lines 12-15). As transistors disposed on integrated circuits become smaller, proper design and engineering of the source/drain extensions becomes critical to the operation of small-scale transistors. (Specification, page 2, lines 17-20). Asymmetrical source and drain extensions, in particular, a drain extension which is deeper than a source extension, provide advantageous transistor performance. (Specification, page 5, line 18 to page 6, line 11).

Claim 18, the representative claim for the first group, is directed to an integrated circuit including a plurality of transistors. Each of the transistors 12 includes a gate structure 18 disposed over a channel 31, a deep source region 22, a deep drain region 24, a source extension 23 and a drain extension 25. The deep source region 22 and the deep drain region 24 are heavily doped with dopants of a first conductivity type. (Figure 1, Specification, page 4, line 23 to page 5, line 3). Source extension 23 is integral to the deep source region 22 and drain extension 25 is integral to the deep drain region 24. Drain extension 25 is deeper than the source extension 23. (Figure 1, Specification, page 5 line 17 to page 6 line 11).

Claim 19, the representative claim of the second group, is dependent from claim 18. Claim 19 includes the additional feature that the source extension 23 is more heavily doped than the drain extension 25.

Claim 26, the representative claim of the third group, is dependent from claim 25. Claim 26 includes the additional feature that the source extension 23 has approximately 5 times the concentration of dopants of the drain extension 25.

Claim 31, the representative claim of the fourth group, is directed to an ultra-large scale integrated circuit including a plurality of transistors. (Specification, page 6, lines 12-14). Each transistor 12 includes a gate structure 12 on a top surface of a semiconductor substrate that is between a deep source region 22 and a deep drain region 24 with dopants of a first conductivity type. (Figure 1, Specification, page 4, line 23 to page 5, line 3). Each

transistor 12 also includes a source extension 23 with dopants of the first conductivity type and a drain extension 25 with dopants of the first conductivity type. The drain extension 25 is deeper than the source extension 23. (Figure 1, Specification, page 5, line 17 to page 6, line 11).

Claim 36, the representative claim of the fifth group, is dependent upon claim 31. Claim 36 includes the additional feature of a unique concentration of dopants associated with the deep source and deep drain regions and the source extension and the drain extension. (Specification, page 4, line 30 to page 5, line 1, page 5, lines 25-26 and page 6, lines 10-11).

ISSUES

1. Whether the claims of Groups 1-5 may properly be rejected under 35 U.S.C. § 103(a) based on Kadosh et al. in view of asserted common knowledge in the art?

GROUPING OF THE CLAIMS

For the purposes of this appeal only, grouping of the claims is as follows:

1. Claims 18, 21-25 and 27-30 essentially stand or fall together and are therefore grouped together. Independent claim 18 is the representative claim for the group because it is the broadest claim in the group.

2. Claims 19 and 20 essentially stand or fall together and are therefore grouped together. Claim 19 depends from claim 18 and includes the additional feature that the source extension is more heavily doped than the drain extension.

3. Claim 26 essentially stands or falls by itself and is therefore grouped by itself. Claim 26 depends on claim 25 and includes the additional feature that the source extension has approximately 5 times the concentration of dopants of the drain extension.

4. Claims 31-35 and 37 essentially stand or fall together and are therefore grouped together. Independent claim 31 is the representative claim for the group because it is the broadest claim in the group.

5. Claim 36 essentially stands or falls by itself and is therefore grouped by itself. Claim 36 depends from claim 31 and includes the additional feature of unique concentrations of dopants associated with the deep source region, the deep drain region, the source extension and the drain extension.

Thus, Appellant respectfully requests individual consideration of each of the five groups herein described. The separate patentability of groups 1-5 is discussed below in the Argument.

ARGUMENT

REFERENCE RELIED UPON

The following reference was relied upon by the Examiner: U.S. Patent No. 5,677,224 to Kadosh et al., issued October 14, 1997.

BRIEF DESCRIPTION OF REFERENCE

U.S. Patent No. 5,677,224 to Kadosh et al. (hereinafter referred to as Kadosh) issued on October 14, 1997. Kadosh teaches a method for making asymmetrical N-channel and P-channel devices. One or both devices include a lightly doped drain region, heavily doped source and drain regions, and an ultra-heavily doped source region. (Kadosh, col. 3, lines 6-10). A heavily doped source region (P+) 204 and a ultra-heavily doped source region (P++) 206 merge to form a source and lightly doped drain region (P-) 152 and heavily doped drain region (P+) 198 merge to form a drain. (Kadosh, Figure 1U, col. 9, lines 40-57). Drain extension 152 is shallower than source extension 204. (Kadosh, Figure 1U). Such a device structure has low source-drain series resistance and reduces hot carrier effects. (Kadosh col. 3, lines 13-15).

BACKGROUND

All claim rejections at issue in this appeal are made under 35 U.S.C. § 103(a)[1] The legal standards under 35 U.S.C. § 103(a) are well-settled.

Obviousness under 35 U.S.C. § 103(a) is a legal conclusion involving four factual inquiries:

(1) the scope and content of the prior art;

(2) the differences between the claims and the prior art;

(3) the level of ordinary skill in the pertinent art; and

(4) secondary considerations, if any, of non-obviousness.

[1] "A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made." 35 U.S.C. §103(a).

Litton Systems, Inc. v. Honeywell, Inc., 87 F. 3d 1559, 1567, 39 U.S.P.Q. 2d 1321, 1325 (Fed. Cir. 196). See also Graham v. John Deere Co., 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

In proceedings before the Patent and Trademark Office (PTO), the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. In re Piasecki, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); Manual of Patent Examining Procedure (MPEP), Edition 8(e8), August 2001, Sections 2142, 2143.03. "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 972 F.2d 1260 (Fed. Cir. 1992); In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988); In re Lalu, 747 F.2d 703,705, 223 U.S.P.Q. 1257, 1258 (Fed. Cir. 1984); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297 n.24, 227 U.S.P.Q. 657, 667 n.24 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 782 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). When a reference teaches away from the claimed invention, that teaching is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Furthermore, proceeding contrary to accepted wisdom is strong evidence of non-obviousness. In re Hedges, 83 F.2d 1038, 228 U.S.P.Q. 685 (Fed. Cir. 1986).

REJECTIONS

1. The claims of Groups 1-5 are patentable under 35 U.S.C. § 103(a) over Kadosh because Kadosh does not teach or suggest the Drain Extension is Deeper Than the Source Extension Limitation.

In paragraphs 2, 3, 4 and 5 of the Final Office Action, the Examiner rejected the claims in Groups 1-5 as being unpatentable under 35 U.S.C. § 103(a) over Kadosh. Each of the independent claims 18, 21, and 31 recites a feature in which the drain extension is deeper than the source extension. This structure provides significant advantages. More particularly, the shallower source extension and deeper drain extension achieves at least three beneficial effects: 1) Substantial immunity to short channel effects; 2) reduced peak electric field in the channel region reduces the possibility of hot-carrier injection into the gate oxide; and 3) higher drive current. (See Specification, page 3, lines 1-10). The shallower source extension allows the transistor to achieve control of short channel effects and higher drive

currents and yet the deeper drain extension allows the transistor to reduce hot carrier injection stress. (See Specification, page 5, line 15 to page 6, line 7).

The Examiner admits that Kadosh does not disclose a drain extension that is deeper than the source extension as required by independent claim 18, 21 and 31. Indeed, Kadosh shows a drain extension that is shallower than the source extension (Kadosh, Figure 1U) However, the Examiner asserts:

> It is well known in the art that a source and drain are identical structures in the device and are only designated by the term "source and drain" to distinguish how the circuit is biased, in which case a source and drain are interchangeable [see Liu et al. (U.S. 6,218,276 B1) in col. 4, lines 29-30].

The Examiner further contends that "it would have been an obvious modification to one of ordinary skill in the art to form the drain extension deeper than the source extension . . . since a drain and source are made of the same materials and only differ because of biasing of the circuit."

As admitted by the examiner, Kadosh clearly does not teach or suggest the limitation that the drain extension that is deeper than the source extension. In addition, contrary to the Examiner's contention, the source and drain are distinct structures which have established meanings to one of ordinary skill in the art and, therefore, it would not be an obvious modification to form a drain extension deeper than the source extension. The terms "source and drain" in the present application are defined in a manner consistent with the IEEE Standard Dictionary of Electrical and Electronics Terms. The IEEE Standard Dictionary of Electrical and Electronic Terms defines the drain as "a region in the device structure of a insulated-gate-field-effect transistor (IGFET) which contains a terminal into which charge carriers flow from the source through the channel. It has the potential which is more attractive than the source for the carriers in the channel." The IEEE Standard Dictionary of Electrical and Electronic Terms defines the source as a "region in the device structure of an insulated-gate-field-effect transistor (IGFET) which contains the terminal from which charged carriers flow into channel toward the drain. It has the potential which is less attractive than the drain for the carriers in the channel." Therefore, the source and drain are distinct structures that have completely distinct functions during the operation of a transistor. In fact, the drain and source have opposite functions as one is a supplier of charge carriers and the other is a receiver of charge carriers. These functions are set by the physical

structure of the device. The integrated circuit includes pins and conductors which are biased to effect the prescribed source and drain functions. The invention as defined by independent claims 18, 21 and 31 is related to the specific function of the source and drain and, therefore, the distinction between the source and drain cannot be ignored.

The Examiner also contends that "...because a source is structurally the same as a drain, any such structure, which is formed by implanted dopants in a substrate on opposing sides of a gate and having a channel in between them, can be designated as either a source or drain." (Final Office Action, page 4, lines 10-13) This position unfairly minimizes the importance of theses structures with respect to the transistor as a whole. Various other integrated circuit (IC) structures are also simply doped regions within a substrate, such as, a channel region or a halo region. Indeed, the halo regions could probably be biased in such a way as to perform in a similar fashion to source and drain regions. This ability to so bias a transistor does not make halo regions interchangeable with source and drain regions.

Further, there is no suggestion in Kadosh to exchange the source extension with the drain extension. Indeed, the specification of Kadosh lists a myriad of alternatives and not one of the alternatives mentions a substitution of the drain extension and the source extension. (Kadosh, col. 10, lines 4-60). The Examiner cites Liu et al (US 6,218,276 at col. 4, lines 29-30) to support the assertion that a source and a drain are interchangeable. Appellant acknowledges that Liu et al. states the terms source and drain are interchangeable (Liu, col. 4, lines 29-30). This statement, however, relates to a symmetric transistor in which the source and drain are identical. While the terms "source and drain" may be interchangeable when the source and drain are in fact the same structure, this is not the case in Kadosh or in the present application. Indeed, the structures in Kadosh and the present application are asymmetric transistor structures where the function of the source and drain are not identical, a point well understood by one of ordinary skill in the art. Further, the statement from Liu et al. does not apply in this case, in which the distinction between the source and drain, as discussed above, cannot be ignored.

As mentioned above, a prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP, Edition 8(e8), August 2001, Sections 2142, 2143.03. Accordingly, the claims of Groups 1-5 are patentable over Kadosh which does not teach or suggest the limitation that a drain extension is deeper than a source extension.

2. The claims of Groups 1-5 are patentable under 35 U.S.C. §103(a) over Kadosh because Kadosh teaches away from the Drain Extension is Deeper than the Source Extension Limitation.

As discussed above in section 1, Kadosh does not disclose or suggest the structure recited in independent claims 18, 21 and 31, in particular, the limitation that the drain extension that is deeper than the source extension. Not only does Kadosh not provide a suggestion for this structure, Kadosh teaches precisely the opposite structure. Specifically, Kadosh shows a drain extension which is shallower than the source extension. (Kadosh, Figure 1U).

Although Kadosh mentions the advantages of lower source-drain series resistance and reduced hot carrier effects, it achieves these advantages by relying on a structure with a lightly doped drain, a heavily doped deep drain, a heavily doped source and ultra-heavily doped deep source. (Kadosh, col. 3, lines 7-15). If one of ordinary skill in the art used Kadosh in pursuit of the advantages mentioned by the Examiner, that person would fabricate an asymmetric transistor with a heavily doped deep drain and an ultra heavily doped deep source. In addition, the source extension would be deeper than the drain extension. Reducing the depth of source extension would not even be considered, especially when Kadosh clearly shows a deeper source extension. (Kadosh, Figure 1U) In addition, as discussed in section 1, it would not have been obvious to one of ordinary skill in the art to interchange the drain and source regions. The source and drain are distinct structures that have completely distinct functions during the operation of a transistor. In particular, an asymmetric transistor structure, as described in Kadosh and the present application, includes a source and drain that are not identical structures and are not interchangeable.

Kadosh clearly teaches away from the claimed invention. As discussed above, teaching away from the claimed invention is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Accordingly, the claims of Groups 1-5 are patentable over Kadosh which teaches away from the invention as recited in the claims of Group 2.

3. The claims of Group 2 are patentable under 35 U.S.C. §103(a) over Kadosh because Kadosh teaches away from the Source Extension is More Heavily Doped Than the Drain Extension Limitation.

Dependent claims 19 and 20 recite a feature wherein the source extension is more heavily doped than the drain extension. Even assuming, *arguendo*, that the Examiner's contention that source and drain extensions are readily interchangeable to meet the limitations in the claims of the present application, Kadosh would disclose the opposite structure than that recited in claim 19. In claim 19, the source extension, the shallower extension, is more heavily doped than the drain extension, the deeper extension. In contrast, Kadosh clearly shows that the deeper extension, the source extension, is more heavily doped than the shallower extension, the drain extension. (Kadosh, Figure 1U, col. 3, lines 26-38)

In addition, Appellant respectfully submits that the Examiner cannot interchange the terms "source" and "drain" in the dependent claim from their modified meaning given by the Examiner in the independent claims. Appellant respectfully submits that the Examiner, without explanation, has used one definition for source and drain in the independent claims and then reverts back to the original meaning of "source" and "drain" to teach the limitations of the dependent claims.

Kadosh teaches the exact opposite structure than that in claims 19 and 20 when the terms "source" and "drain" are interchanged as set forth by the Examiner. As mentioned above, Kadosh teaches the deeper extension, the source extension, is more heavily doped than the shallower extension, the drain extension. If the terms "source" and "drain" were interchanged in Kadosh as suggested by the Examiner, Kadosh would teach the deeper extension, the drain extension, is more heavily doped than the shallower extension, the source extension. In contrast, claim 19 recites a structure where the shallower extension, the source extension, is more heavily doped than the deeper extension, the drain extension. Therefore, Kadosh is clearly teaching the opposite of the structure recited in claims 19 and 20.

Teaching away from the claimed invention is strong evidence of non-obviousness. See U.S. v. Adams, 383 U.S. 39, 148 U.S.P.Q. 79 (1966); In re Royka, 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Accordingly, the claims of Group 2 are patentable over Kadosh which teaches away from the structure of the present application where the source extension, the shallower extension, is more heavily doped than the drain extension.

4. The claims of Group 2 are patentable under 35 U.S.C. §103(a) over Kadosh because the Source Extension is More Heavily Doped Than the Drain Extension Limitation is contrary to conventional wisdom.

As discussed in section 3, dependent claims 19 and 20 recite a feature wherein the source extension is more heavily doped than the drain extension. In claim 19, the source extension, the shallower extension, is more heavily doped than the drain extension, the deeper extension. In contrast, Kadosh clearly shows that the deeper extension, the source extension, is more heavily doped than the shallower extension, the drain extension. (Kadosh, Figure 1U, col. 3, lines 26-38) There is no suggestion in Kadosh to make the shallower extension more heavily doped, in fact, such a feature is in contrast to conventional wisdom, conventional wisdom which is embodied in Kadosh. Conventional wisdom for doping extensions of a transistor is that deeper extensions are more heavily doped. In the present application, a shallow, heavily doped source extension provides better control of short-channel effects and reduces current degradation due to series resistance. (Specification, page 5, lines 18-23 and page 8, lines 21-26) In addition, a deeper, lightly doped drain extension provides better reliability under hot-carrier injection stress. (Specification, page 6, lines 6-9 and page 8, lines 28-31)

Proceeding contrary to conventional wisdom is strong evidence of non-obviousness. In re Hedges, 83 F.2d 1038, 228 U.S.P.Q. 685 (Fed. Cir. 1986). Accordingly, the claims of Group 2 are patentable over Kadosh because the claims of Group 2 are contrary to the conventional wisdom as embodied by Kadosh.

5. The claim of Group 3 is patentable under 35 U.S.C. §103(a) over Kadosh because Kadosh does not teach or suggest the Dopants Ratio Between the Source Extension and the Drain Extension is Approximately Five Limitation.

Dependent claim 26 recites the limitation that the ratio of dopants between the source extension and the drain extension is approximately five. Even assuming, *arguendo*, that the Examiner's contention that source and drain extensions are readily interchangeable to meet the limitations in the claims of the present invention, Kadosh does not teach or suggest the limitation required by claim 26. In contrast, Kadosh discloses that the dopant concentration of the heavily doped source region is in the range of 10 to 100 times that of the lightly doped drain region. (Kadosh, col. 3 lines 29-33). Clearly the ratio of doping between the source and drain extensions in Kadosh is different than that as claimed in dependent

claim 26. Further, there is no suggestion to reduce the doping ratio of Kadosh by 2–20 times to provide the ratio as required in dependent claim 26 of the present invention.

A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP, Edition 8(e8), August 2001, Sections 2142, 2143.03. Accordingly, the claim of group 3 is patentable over Kadosh, which does not teach or suggest a ratio of dopants between the source extension and the drain extension of approximately five.

6. The claim of Group 5 is patentable under 35 U.S.C. §103(a) over Kadosh because Kadosh does not teach or suggest the dopant concentration limitations as recited in the claim of Group 5.

Dependent claim 36 recites a unique concentration of dopants associated with the deep source and deep drain regions and the source extension and the drain extension. In particular, claim 36 requires that the deep source region and the deep drain region have the same dopant concentrations and that the source extension, the shallow extension, has a higher concentration of dopants than the drain extension, the deeper extension. Even assuming, *arguendo*, that the Examiner's contention that source and drain extensions are readily interchangeable to meet the limitations in the claims of the present application, Kadosh does not teach or suggest the limitations of claim 36. In contrast, Kadosh teaches the use of a deep source region having a different concentration of dopants than the deep drain region and a source extension, the deeper extension, having a higher concentration of dopants than a drain extension, the shallower extension. (Kadosh, Figure 1, col. 3, lines 29-33) There is simply no suggestion for altering the concentration of dopants in Kadosh to meet the limitations of claim 36.

A prima facie case of obviousness requires that the prior art reference or references teaches or suggests all of the claimed limitations. See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974); MPEP, Edition 8(e8), August 2001, Sections 2142, 2143.03. Accordingly, the claim of group 5 is patentable over Kadosh which does not teach or suggest the dopant concentration limitations as recited in claim 36.

CONCLUSION

In view of the foregoing, the Appellant submits that the claims are not properly rejected as being unpatentable under 35 U.S.C. § 103(a) under the cited reference. Accordingly, it is respectfully requested that the board reverse the claim rejections and indicate that a Notice of Allowance respecting all pending claims be issued.

Dated this 23rd day of October, 2002

Respectfully submitted,

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APPENDIX - THE CLAIMS ON APPEAL

18. An integrated circuit including a plurality of field effect transistors, each of the transistors comprising:

a gate structure disposed over a channel;

a deep source region heavily doped with dopants of a first conductivity type;

a deep drain region heavily doped with dopants of the first conductivity type;

a source extension integral the deep source region; and

a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension.

19. The integrated circuit of claim 18, wherein the source extension is more heavily doped that the drain extension.

20. The integrated circuit of claim 19, wherein the drain extension is more than 80 nm thick and the source extension is less than 40 nm thick.

21. An integrated circuit includes a gate structure disposed over a channel, a deep source region heavily doped with dopants of a first conductivity type, a deep drain region heavily doped with dopants of the first conductivity type, a source extension integral the deep source region, and a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension, wherein the integrated circuit is manufactured by a method, comprising:

providing the gate structure between a source location and a drain location in a semiconductor substrate;

providing an angled source extension implant in a direction from the source location to the drain location;

providing an angled drain extension implant in a direction from the drain location to the source location; and

providing a deep source/drain implant at the source location and the drain location.

22. The integrated circuit of claim 21, further comprising providing a pair of spacers abutting lateral sides of the gate structure before the deep source drain implant.

23. The integrated circuit of claim 22, wherein the providing the source extension step is a low energy, high dose ion implantation step.

24. The integrated circuit of claim 23, wherein the drain extension implant step is a medium energy, high dose ion implantation step.

25. The integrated circuit of claim 24, wherein a source extension formed by the source extension step is shallower than a drain extension formed by the drain extension implant step.

26. The integrated circuit of claim 25, wherein the source extension has approximately 5 times the concentration of dopants of the drain extension.

27. The integrated circuit of claim 25, wherein the source extension has a concentration of $5x10^{19}$-$1x10^{20}$ of dopants per centimeter cubed and the drain extension has a concentration of $1x10^{19}$-$5x10^{19}$ dopants per centimeter cubed.

28. The integrated circuit of claim 25, wherein the drain extension has a concentration between $1x10^{19}$-$5x10^{19}$ dopants per centimeter cubed.

29. The integrated circuit of claim 25, wherein the drain extension is more than 80 nm deep.

30. The integrated circuit of claim 27, wherein the gate structure is associated with a N-channel or P-channel with MOSFET.

31. An ultra-large scale integrated circuit including a plurality of field effect transistors, the field effect transistors comprising:

a gate structure on a top surface of a semiconductor substrate;

a source extension with dopants of a first conductivity type;

a drain extension with dopants of the first conductivity type; and

deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.

32. The integrated circuit of claim 31, further comprising:
a pair of spacers abutting lateral sides of the gate structure.

33. The integrated circuit of claim 31, wherein the drain extension is formed in a low dosage implant process.

34. The integrated circuit of claim 31, wherein the source extension is formed at an energy level of between 1-5 KeV.

35. The integrated circuit of claim 31, wherein the drain extension is formed at an energy level of between 5-15 KeV.

36. The integrated circuit of claim 31, wherein the deep source and deep drain regions have a concentration of dopants between 10^{19} and 10^{20} dopants per cc, the source extension has a concentration of dopants between $5x10^{19}$ and 10^{20} dopants per cc, and the drain extension has a concentration of dopants between $1x10^{19}$ and $5x10^{19}$ dopants.

37. The integrated circuit of claim 31, wherein the first conductivity type is P-type or N-type.